IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:		ATTORNEY FILE NO.:
Inventors:	Ono et al.	SLA0830
Serial No.:	10/805,158	Examiner: Pizarro-Crespo, Marcos
Filed:	March 19, 2004	Customer No.: 55,286
Title:	CHARGE TRAP NON-VOLATILE MEMORY STRUCTURE FOR 2 BITS PER TRANSISTOR	Group Art: 2814
		Confirmation No.: 8642

Board of Patent Appeals and Interferences
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

BRIEF ON APPEAL

This is an appeal from the rejection by Examiner Marcos Pizarro-Crespo, Group Art Unit 2814, of claims 16-17 and 20-28 as set forth in the CLAIMS APPENDIX, all claims in the application.

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REAL PARTY IN INTEREST

The real party in interest is Sharp Laboratories of America, Inc., as assignee of the present application by an Assignment in the United States Patent Office, with a recordation date of March 19, 2004 at Reel 015123, Frame 0830.

RELATED APPEALS AND INTERFERENCES

None.

STATUS OF THE CLAIMS

Claims 1-15 and 18-19 are canceled.

Claims 16-17 and 20-28 are in the application.

Claims 16-17 and 20-28 are rejected.

Claims 16-17 and 20-28 are appealed.

STATUS OF AMENDMENTS

Amendments to the claims were made in an Office Action response filed on February 8, 2006. These claim amendments have been entered.

SUMMARY OF CLAIMED SUBJECT MATTER

Generally, the invention is a type of non-volatile memory transistor. Conventionally, a charge (memory state) can be stored in a transistor gate stack by using either a conductive charge trapping layer (floating gate), or more preferably, a non-conductive charge trapping layer, which is made from either a silicon nitride or oxide/nitride/oxide (ONO) stack. The use of silicon nitride can (undesirably) lead to lateral

diffusion of charge, while the oxide in an ONO stack must be of a high quality, and therefore, difficult to fabricate. Additional details describing conventional non-volatile memory transistors can be found in the Applicant's specification (page 1, line 8, through page 3, line 21; see Fig. 1).

Claim 16 describes a method for fabricating a non-volatile memory transistor. The transistor comprises a gate stack with a single layer of high-k dielectric material underlying the gate electrode. Charge trapping centers are formed in the high-k dielectric in response to being exposed to an ionized species. Claim 16 specifically recites that there is no oxide layer underlying the high-k dielectric, and no oxide layer overlying the high-k dielectric. Details of the process can be found in the specification at page 5, line 9, through page 7, line 24, and at page 9, lines 9-18 (see Fig. 2).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Whether claims 16-17, 20-22, and 25-27 are unpatentable under 35 U.S.C. 103(a) with respect to Halliyal (US 6,451,641), in view of King (US 6,754,104) and Kirkpatrick (US 4,197,144).

2. Whether 23 is unpatentable under 35 U.S.C. 103(a) with respect to Halliyal, King, and Kirkpatrick, and further in view of Chooi (US 6,486,080) and Agarwal (US 2001/0015453).

3. Whether claim 24 is unpatentable under 35 U.S.C. 103(a) with respect to Halliyal, King, and Kirkpatrick, and further in view of Liang (US 5,372,957).

4. Whether claim 28 is unpatentable under 35 U.S.C. 103(a) with respect to Halliyal, King, and Kirkpatrick, and further in view of Moslehi (US 5,372,957).

ARGUMENT

1. The rejection of claims 16-17, 20-22, and 25-27 as unpatentable under U.S.C. 103(a) with respect to Halliyal (US 6,451,641), in view of King (US 6,754,104) and Kirkpatrick (US 4,197,144).

In Section 4 of the Office Action claims 16-17, 20-22, and 25-27 have been rejected under 35 U.S.C. 103(a) as unpatentable with respect to Halliyal, in view of King and Kirkpatrick. Regarding claim 16, the Office Action acknowledges that Halliyal does not describe the steps of inducing trapping centers in a dielectric material, in response to an ionized species exposure. The Office Action also states that it would have been obvious at the time of the invention to induce trapping centers into a dielectric material, as suggested by King and Kirkpatrick, to increase the number of storage sites within the dielectric layer.

An invention is unpatentable if the differences between it and the prior art would have been obvious at the time of the invention. As stated in MPEP § 2143, there are three requirements to establish a *prima facie* case of obviousness.

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference

> teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck* 947 F.2d 488, 20 USPQ2d, 1438 (Fed. Cir. 1991).

Halliyal generally describes a MOS transistor made with a high-k dielectric (Abstract). The novelty of Halliyal's invention appears to be a method of forming a polySi gate electrode that does not "reduce" the underlying high-k dielectric gate insulator (col. 5, ln. 27-46). Halliyal does not describe either a NROM or MONOS memory device, or any kind of transistor that operates on a charge trapping or floating gate principle. More particularly, Halliyal does not describe the steps of exposing a high-k dielectric material to an ionized species, inducing charge trapping centers in the high-k dielectric material as a result of the exposure, or a device where charge can be trapped in a gate stack.

Generally, King discloses processes for forming an integrated gate FET (IGFET) and a negative differential resistance (NDR) FET using common processing operations (Abstract). King states that a first electrically insulating layer 1020 (e.g., a high permittivity dielectric) is formed over a substrate. King states that it is desirable to induce trapping centers in the insulating layer 1020, by ion implantation or diffusion (col. 14, ln. 4-20). Ions such as boron, indium, arsenic, phosphorus, fluorine, chlorine, or germanium are selectively implanted in either the substrate, or into the areas where the FETS are to be formed (col. 14, ln. 31-51).

The ***Response to Arguments*** Section of the Office Action states that King describes a memory cell, citing col. 8, ln. 56-60. However,

the cited section states that "a bistable memory device can be obtained when an NDR-FET and IGFET are formed on the same semiconductor substrate. Data can be written or read from such cell 100 in any conventional fashion..." As is well known the art, a bistable memory cell is a multi-transistor circuit that stores a memory state in the form of a voltage. King notes that his bistable memory cell 100 consists of a pull-up element (e.g., IGFET 110) and a pull-down element (e.g., NDR-FET 120) (col. 7, ln. 64, - col. 8, ln. 3). In other words, the IGFET and NDR-FET transistors, as individual elements, do have a charge storage capability.

As noted in the affidavit accompanying this response, it is the opinion of Dr. David R. Evans that King uses change trapping for the purpose of inducing a negative differential resistance, and that King's charge trapping centers cannot be used for non-volatile purposes. That is, King's NDR FET does not store a memory state (charge).

Generally, Kirkpatrick discloses an ion implantation process for forming charge trapping sites into an insulator material. Kirkpatrick notes that a memory can be enabled by reading charge storage variations in the oxide electrode insulator of a planar *diode* structure (col. 1, ln. 11-31). Kirkpatrick explicitly describes such a diode device having a pn junction 11/12, an oxide layer 14, and a conductive electrode layer 15. At col. 4, ln. 5, Kirkpatrick discloses implanting a silicon dioxide insulator with Si ions. Unlike the claimed invention, which recites forming charge trapping centers in a high-k dielectric, Kirkpatrick discloses a silicon dioxide insulator. Unlike, the claimed invention, which recites a transistor memory device, Kirkpatrick discloses a diode memory.

With respect to the first *prima facie* requirement, there must be some suggestion in the King and Kirkpatrick references to modify

Halliyal in a manner that makes the claimed invention obvious. The Office Action states that it would have been obvious to combine the references, to increase the number of storage sites within the dielectric layer. However, the Applicant respectfully submits that such a rationale can only be constructed in hindsight, in light of the claimed invention. That is, it appears as if the references were chosen as a result of a search using limitations from the claimed invention as keywords. No evidence has been provided of particular features from either the King or Kirkpatrick disclosures that would suggest modifications to Halliyal.

Kirkpatrick is the only reference that specifically mentions a memory application. No evidence has been provided in the Office Action that an expert in the art would be motivated to modify a process that protects a high-k dielectric from reduction (Halliyal), in light of a NDR FET or a memory diode, to increase the number of storage sites in a dielectric layer, as suggested in the Office Action. On its face this assertion is flawed because Halliyal discloses no storage sited in the first place. Alternately stated, it is not logical to base the rejection of the Applicant's memory transistor upon a primary reference that is not itself a memory device. Further, no evidence has been provided that an expert would seek to modify Halliyal's transistor in such a manner as to make a memory transistor.

The legal concept of *prima facie* obviousness is a procedural tool of examination which applies broadly to all arts. It allocates who has the burden of going forward with production of evidence in each step of the examination process. See *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *In re Linter*, 458 F.2d 1013, 173 USPQ 560 (CCPA 1972); *In re Saunders*, 444 F.2d 599, 170 USPQ 213 (CCPA 1971); *In re*

Tiffin, 443 F.2d 394, 170 USPQ 88 (CCPA 1971), *amended*, 448 F.2d 791, 171 USPQ 294 (CCPA 1971); *In re Warner*, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967), *cert. denied*, 389 U.S. 1057 (1968).

The CAFC has consistently found over the years that a *prima facie* case for obvious must be based upon a detailed analysis of how and why an expert could excerpt known art to make modifications to a cited prior art reference. In other words, the examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art reference for combination in the manner claimed." *In re Rouffet*, 47 USPQ2d 1453, 1457-1458 (1998).

In the present case, the Office Action states that it would have been obvious to combine the teachings of King and Kirkpatrick with Halliyal, "to increase the number of storage sites within the dielectric layer." The Applicant submits that this statement is insufficient to support a *prima facie* case of obviousness.

Considered from the perspective of the second *prima facie* requirement, even if an expert were given the three references as a foundation, there is no reasonable expectation that this expert could derive the claimed invention, since none of the references suggest the claimed gate stack structure. That is, none of the reference discloses a memory transistor with charge trapping region formed from a single layer of high-k dielectric (without an underlying or overlying oxide layer).

With respect to the third *prima facie* requirement, even if the references are combined, they do not disclose all the elements of the claimed invention. Applicant's claim 16 recites the steps of forming a gate stack with a single layer of a charge trapping high-k dielectric, without

underlying/overlying oxide insulator layers. As noted above, Halliyal does not address the subject of charge trapping or of a memory FET. King does not address the use of charge traps for memory applications. Kirkpatrick does not describe a transistor memory or a high-k dielectric material. Therefore, the combination of references does not explicitly describe all the steps of claim 16. Neither does the combination of references suggest any modifications that make these limitations obvious. Claims 17, 20-22, and 25-27, dependent from claim 16, enjoys the same distinctions from the cited prior art.

2. The rejection of claim 23 as unpatentable under U.S.C. 103(a) with respect to Halliyal, King, and Kirkpatrick, and further in view of Chooi (US 6,486,080) and Agarwal (US 2001/0015453) .

In Section 14 of the Final Office Action claim 23 has been rejected under 35 U.S.C. 103(a) as unpatentable with respect to Halliyal, King, and Kirkpatrick, and further in view of Chooi and Agarwal. The Office Action acknowledges that Halliyal/King/Kirkpatrick do not describe a densification annealing, but that Chooi and Agarwal do. The Office Action states that it would have been obvious to follow the deposition of the Halliyal/King/Kirkpatrick trapping layer with an annealing to cure oxygen vacancies.

At col. 6, ln 5-7, Chooi describes the densification of a metal oxide. At paragraph [0005] Agarwal describes densification to cure oxygen vacancies in a high-k dielectric. It is not clear how these references have any application to the claimed invention, which performs a densification annealing to prevent delamination of the gate

(specification, page 12, ln. 24-25). Further, neither of these references describes ion implantation processes, the use of a high-k dielectric as a charge trapping material, or the use of a high-k dielectric memory device. These references do not suggest any modifications to the King/Kirkpatrick ion implantations. Likewise, these references do not suggest modifications to Halliyal's high-k dielectric reduction protection process. No evidence has been provided in the Final Office Action to support these assumptions, and the Applicant respectfully submits that a *prima facie* case has not been made to combine the prior art references.

With respect to the third *prima facie* requirement, even if the references are combined, they do not disclose all the elements of the claimed invention. Applicant's claim 16 recites forming a gate stack with a single layer of a charge trapping high-k dielectric, without underlying/overlying oxide insulator layers. None of the references explicitly describes these steps. The addition of Chooi and Agarwal to the combination of references still suggests no modifications that would make these limitations obvious. Claim 23, dependent from claim 16, enjoys the same distinctions from the cited prior art.

3. The rejection of under 35 U.S.C. 103(a) as unpatentable with respect to Halliyal, King, and Kirkpatrick, and further in view of Liang (US 5,372,957).

In Section 16 of the Final Office Action claim 24 has been rejected under 35 U.S.C. 103(a) as unpatentable with respect to Halliyal, King, and Kirkpatrick, and further in view of Liang. The Office Action acknowledges that Halliyal/King/Kirkpatrick do not describe a drain/source angle implant, as described by Liang. The Office Action

states that it would have been obvious to form Halliyal's source/drain regions using Liang's process, to protect the transistor from hot carrier degradation.

Even if Liang does describe an angle implant to form source/drain regions, it is not apparent that Liang suggests any modifications to the ion implantation processes of either King or Kirkpatrick, or to Halliyal's high-k dielectric reduction protection process. No evidence has been provided in the Final Office Action to support this assumption, and the Applicant respectfully submits that a *prima facie* case has not been made to combine the prior art references.

With respect to the third *prima facie* requirement, the combination of references does not disclose all the elements of the claimed invention. Applicant's claim 16 recites forming a gate stack with a single layer of a charge trapping high-k dielectric, without underlying/overlying oxide insulator layers. None of the references explicitly describes these steps. Neither does the combination of references suggest any modifications that make these limitations obvious. Claim 24, dependent from claim 16, enjoys the same distinctions from the cited prior art.

4. The rejection of claim 28 under 35 U.S.C. 103(a) as unpatentable with respect to Halliyal, King, and Kirkpatrick, and further in view of Moslehi (US 5,372,957).

In Section 18 of the Final Office Action claim 28 has been rejected under 35 U.S.C. 103(a) as unpatentable with respect to Halliyal, King, and Kirkpatrick, and further in view of Moslehi. The Office Action

acknowledges that Halliyal/King/Kirkpatrick do not describe generating plasma using an ICP source, as described by Moshehi.

Again, no evidence has been provided in the Final Office Action to support the assumption that an expert would seek to modify the Halliyal/King/Kirkpatrick references using an ICP generated plasma, and the Applicant respectfully submits that a *prima facie* case has not been made to combine the prior art references. However, even if the above-mentioned references can be combined, they do not disclose all the elements of the claimed invention. With respect to the third *prima facie* requirement, Applicant's claim 16 recites forming a gate stack with a single layer of a charge trapping high-k dielectric, without underlying/overlying oxide insulator layers. None of the references explicitly describes these steps. Neither does the combination of references suggest any modifications that make these limitations obvious. Claim 28, dependent from claim 16, enjoys the same distinctions from the cited prior art.

SUMMARY AND CONCLUSION

It is submitted that for the reasons pointed out above, the claims in the present application clearly and patentably distinguish over the cited references. Accordingly, the Examiner should be reversed and ordered to pass the case to issue.

The fee for filing this Appeal Brief is enclosed. Authorization is given to charge any deficit or credit any excess to Deposit Account No. 502,033.

Respectfully submitted,

Date: 11/15/2006

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TABLE OF CONTENTS

CLAIMS APPENDIX

1-15. canceled

16. (previously presented) A method of fabricating a non-volatile memory transistor comprising the steps of:

preparing a semiconductor substrate;

forming a gate stack on the substrate, as follows:

depositing a single layer of high-k dielectric material, without an underlying oxide insulator layer and an overlying oxide insulator layer;

exposing the high-k dielectric material to an ionized species;

in response to the ionized species exposure, inducing trapping centers in the high-k dielectric material; and

forming an electrode layer overlying the high-k dielectric with the charge trapping centers; and

forming drain and source regions on opposite sides of the gate stack.

17. (original) A method as in claim 16 wherein the high-k dielectric material comprises at least one of aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), zirconium oxide (ZrO_2), titanium oxide (TiO_2), tantalum oxide (Ta_2O_5), cesium oxide (CeO_2), lanthanum oxide (La_2O_3), tungsten oxide (WO_3), yttrium oxide (Y_2O_3), bismuth silicon oxide ($Bi_4Si_2O_{12}$), barium strontium oxide ($Ba_{1-x}Sr_xO_3$), lanthanum aluminum oxide ($LaAlO_3$), hafnium silicate ($HfSiO_4$), zirconium silicate ($ZrSiO_4$), aluminum hafnium oxide (AlHfO), aluminum oxynitride (AlON), hafnium

silicon oxynitride (HfSiON), zirconium silicon oxynitride (ZrSiON), barium titanate ($BaTiO_3$), strontium titanate ($SrTiO_3$), lead titanate ($PbTiO_3$), barium strontium titanate (BST) ($Ba_{1-x}Sr_xTiO_3$), lead zirconium titanate, lead lanthanum titanate, bismuth titanate, strontium titanate, lead zirconium titanate (PZT ($PbZr_xTi_{1-x}O_3$)) barium zirconium titanate, strontium bismuth tantalate, lead zirconate ($PbZrO_3$), PZN ($PbZn_xNb_{1-x}O_3$), PST ($PbSc_xTa_{1-x}O_3$), or PMN ($PbMg_xNb_{1-x}O3$).

18-19. canceled

20. (previously presented) A method as in claim 16 wherein exposing the high-k dielectric material to the ionized species includes exposing the high-k dielectric to a species selected from the group consisting of oxygen, nitrogen, and hydrogen.

21. (previously presented) A method as in claim 16 wherein exposing the high-k dielectric material to the ionized species includes exposing the high-k dielectric material to a plasma for an exposure time in the range of about 10 seconds and 100 seconds.

22. (previously presented) A method as in claim 16 wherein depositing the high-k dielectric material includes depositing using an ALD method.

23. (previously presented) A method as in claim 16 further comprising a densification anneal step after the deposition of the high-k dielectric material.

24. (original) A method as in claim 16 wherein the formation of the drain and source regions comprises an angle source and drain implantation.

25. (previously presented) A method as in claim 16 wherein the semiconductor substrate is selected from a group consisting of SOI substrate, bulk silicon substrate, and insulator substrate.

26. (original) A method as in claim 16 wherein the memory transistor is a multi-bit memory transistor.

27. (previously presented) A method as in claim 16 wherein exposing the high-k dielectric material to an ionized species includes using an ion energy in the range of about 10 to 300 keV and a dose in the range of about 1×10^{14} to 1×10^{17}.

28. (previously presented) A method as in claim 16 wherein exposing the high-k dielectric material to an ionized species includes generating a plasma using an inductively coupled plasma (ICP) source.

EVIDENCE APPENDIX

DECLARATION OF DAVID R. EVANS UNDER 37 CFR §1.132

I, David Russell Evans, Ph.D., hereby declare as follows:

1. My residence address is 7574 S.W. 179th Street, Beaverton, Oregon 97007.

2. Since April 1, 1999 I have been employed by Sharp Laboratories of America, Inc. ("SLA"), 5700 N.W. Pacific Rim Boulevard, Camas, Washington 98607, and between 1993 and April 1, 1999 I was employed by SLA's predecessor company, Sharp Microelectronics Technology, Inc. ("SMT"), located at the same address. My titles at SMT (until April 1, 1999) were, originally, Principal Engineer and, later, Senior Member of the Technical Staff, and my title at SLA, since April 1, 1999, is Senior Manager. My responsibilities include developing advanced process technologies to improve microelectronics fabrication. My technical experience is detailed in the accompanying CV.

3. I have read the claims for the patent application in question, Ono et al., Serial Number 10/805,158 (the Applicant), entitled "Charge Trap Non-Volatile Memory Structure for 2 Bits per Transistor". I have read the Office Action dated March 10, 2006, where claims 16, 17, 20-22, and 25-27 have been rejected as obvious by Halliyal (US 6,451,641), in view of King (US 6,754,104) and Kirkpatrick (US 4,197,144). I have also reviewed the Chooi (US 6,486,080), Agarwal (US 2001/0015453), Liang (US 5,372,957), and Moslehi (US 5,846,883) references cited by the Examiner.

4. The Examiner, on page 4, claims that Halliyal describes all the steps of claim 16, except for the step of inducing trapping centers in a dielectric material. The Examiner further claims that it would have been obvious to one of ordinary skill in the art to induce trapping centers into the dielectric material by exposing the dielectric to an ionized species, as suggested by King and Kirkpatrick, to increase the number of storage sites within the dielectric layer.

5. As explained in the Applicant's specification (pages 1-3), there exist two fundamental non-volatile memory device types: they are floating gate and NROM devices. The floating gate design uses a conductive charge trapping layer, and is not especially relevant to this discussion. The NROM design uses an oxide/nitride/oxide (ONO) structure, interposed between a gate electrode and a FET channel region, where the nitride layer is a non-conductive charge trapping layer. The tradeoff between oxide quality and oxide thickness has encouraged some manufacturers to replace the ONO oxide layers with high-k insulating materials. The Applicant's invention simplifies the problem by replacing the entire ONO structure with a single (non-conductive) high-k dielectric charge trapping layer. Insulating layers are not needed between the Applicant's charge trapping channel and the channel. Neither is an insulator needed between the charge trapping layer and the gate electrode.

6. Halliyal describes a conventional FET made with a high-k dielectric. Halliyal does not describe charge trapping, or the use of a FET as a memory. Halliyal's high-k dielectric cannot store a charge. Halliyal is concerned with depositing polysilicon or silicon-germanium in a manner that does not damage a high-k dielectric. I see no correlation between the Applicant's memory device and Halliyal's FET process.

7. King describes a number of different embodiments that use the combination of a depletion-mode insulated-gate FET (IGFET) and a negative differential resistance (NDR) FET. An IGFET is a conventional FET device. In column 14, King describes the formation of a first electrical insulating layer 1020, with charge traps at or near the interface to the Si substrate 1000. A second (gate) insulator layer 1040 is formed over the first insulator layer 1020, and King describes techniques for forming charge traps in the gate oxide layer (column 14, line 55 through column 15, line 14).

While King does describe the formation of charge traps in an insulator material, such as a high-k dielectric, it is important to understand that these charge trap regions have nothing to do with non-volatility. Rather, King uses his charge traps to create a negative differential resistance (NDR). I see no crossover between NDR and non-volatile memory applications.

8. Kirkpatrick describes a PIN diode device that can be used as a memory because of charge traps formed in the insulator (I) between the PN junction. The insulator is SiO2, and the trapping sites are formed by implanting Si ions.

9. The Examiner's rationale for combining these three references is not clear to me. Of the three references, only one reference (Kirkpatrick) describes a memory device. Unlike the Applicant's invention, Kirkpatrick describes a diode active device with trapping centers in the SiO2 insulator between the P and N regions. The Applicant does not describe a SiO2 insulator, an insulator between P and N regions, or a diode active device. It appears to me that the Examiner could not have found a memory device that is more different from the Applicant's device than Kirkpatrick's.

Of the three primary prior art references presented by the Examiner, the Halliyal and King references seem even more distant from the Applicant's. While the King and Halliyal devices both use a high-k dielectric, neither of these devices can be used for a non-volatile memory. While King describes a high-k dielectric gate oxide with charge trapping centers, King's charge trapping centers cannot hold a charge or store a memory state.

In summary, I can find no apparent reason for an expert in the art to combine three such disparate references as the King, Halliyal, and Kirkpatrick references. Further, I can unequivocally state that this combination does not suggest a memory transistor invention. Even further, the combination of references does not suggest a memory transistor that is able to replace the conventional ONO structure with the high-k dielectric charge trapping region described by the Applicant.

10. In reviewing the other rejections made in view of the Chooi, Agarwal, Liang, and Moslehi references, I note that even if it would have been obvious to add the features cited in these supplemental references, the combination of any or all of these references with Halliyal/King/Kirkpatrick still fails to suggest a device with all the features described in Applicant's claim 16. For example, with respect to claim 28, even if it would have been obvious to use Moslehi's ICP source in combination with Halliyal/King/Kirkpatrick, that combination would not suggest a non-volatile memory transistor made with a high-k gate dielectric, without underlying or overlying oxide layers, where charge trapping centers are formed in the high-k dielectric. Likewise, the

addition of Liang's angled implantation, or Chooi/Agarwal's densification annealing, even when combined with Halliyal/King/Kirkpatrick, does not describe the features of Applicant's claim 16. Therefore, I do not consider these supplemental references particular relevant to the issue of whether the Applicant's invention is obvious.

11. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful, false statements may jeopardize the validity of the application or any patent issuing thereon.

31 July 2006
Date

David R. Evans

David Russell Evans

Professional Education:

1981 Ph. D. in Physical Chemistry, Iowa State University, Ames, Iowa. Dissertation: "A Comparative Study of Classical and Quantal Approaches to Thermal and Diffusive Transport in a Dilute Atom-Diatom Binary Mixture"

1974 B. S. in Chemistry, Summa Cum Laude, (GPA 3.98) University of Missouri-Rolla, Rolla, Missouri.

Employment History:

5/1999 - Present

Sr. Manager, Dept. 5, SHARP Laboratories of America, Inc.

Responsible for project management and technical guidance of advanced resistive memory project. Previously, directed CVD copper interconnect research and development. In addition, manage chemical synthesis and associated material development. Directly responsible for advanced CMP research directed toward novel device structures, advanced perovskite materials, noble metals, nanostructures, and sensors.

5/1994 – 5/1999

Sr. Member of Technical Staff, Process Technology Laboratory, SHARP Microelectronics Technology, Inc.

Major responsibility was research and development of chemical mechanical polishing (CMP) of copper for advanced interconnect and dielectric materials for shallow trench isolation and related device structures.

11/1988 - 5/1994

Principal Engineer, Integrated Circuit Operations, Tektronix, Inc.

Major responsibility was thin film development and manufacturing, primarily for use as diffusion barriers and thin film resistors.

11/1986 - 11/1988

Principal Engineer, Liquid Crystal Strategic Program Unit, Tektronix, Inc.

Major responsibility was large area photolithography for optical shutters and passive matrix flat panel displays.

10/1980 - 11/1986

Sr. Development Engineer, Bipolar Process Development Dept., Tektronix, Inc.

Major responsibility was plasma etching and deposition. Implemented the first plasma etch processes for integrated circuit fabrication in Tektronix.

Teaching Experience:

9/1994 – 10/2004

Adjunct Faculty-Oregon Graduate Institute of Oregon Health and Science University

Graduate level course, Microelectronics Fabrication I, ECE 560, during fall term: The course covers semiconductor materials, crystal structure and growth, thermal oxidation, ion implantation and diffusion. It is part of a one-year sequence in semiconductor processing that typically is taken both by matriculating graduate students from and working professionals drawn from local industry.

3/1981 – 5/1981

Instructor-Iowa State University

Undergraduate level course, Physical Chemistry: The course covered chemical reaction kinetics, kinetic theory of gases, transport theory, x-ray diffraction and crystal structure. Prepared all lectures and exams.

Refereed Journal and Proceedings Publications:

David R. Evans and Michael R. Oliver, Chemical Mechanical Planarization-Integration, Technology and Reliability, Mater. Res. Soc., PV-867, Warrendale, PA, pg. 189, 2005 (invited). "Abrasive Contribution to CMP Friction"

Parshuram B. Zantye, S. Mudhivarthi, Ashok Kumar, and David Evans, , Chemical Mechanical Planarization-Integration, Technology and Reliability, Mater. Res. Soc., PV-867, Warrendale, PA, pg. 75, 2005. "In-situ Metrology for End Point Detection during Chemical Mechanical Polishing of Shallow Trench Isolation Structure"

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D. R. Evans, J. S. Flores, and S. Dottarar, **4,732,865**, Mar. 22, 1988. "Self-aligned Internal Mobile Ion Getter for Multi-layer Metallization on Integrated Circuits"

Continuing Education and Other Skills:

Broad experience related to collaborative research and development efforts with universities, government laboratories, and private companies. This includes writing legally binding contracts and statements of work, administering grants, and managing collaborative efforts of a more informal nature.

Taken several electrical engineering courses through Oregon State University, Portland State University, and University of Portland that cover fundamental circuits and devices. Additionally, have participated in several work-related technical and management training programs.

Proficient in applied mathematics and algorithm construction.

RELATED PROCEEDINGS APPENDIX

NONE